REMARKS

Favorable reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

No claims have been canceled or added by this amendment. Claims 1-9 are pending in the present application, of which claims 1 and 4 are independent.

Claim Rejection Under 35 U.S.C. §101

Claims 4-9 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Page 2 of the Office Action states that the "Examiner strongly encourages Applicant to amend this claims by adding a specific hardware element (i.e., processor, physical network card, etc.) from the original specification into the body of the claims." As suggested, claim 4 has been amended to include "a PLL circuit", which is supported by the original specification. Claims 5-9 depend from claim 4.

In view of the foregoing discussion, withdrawal of the rejection to claims 4-9 is respectfully requested.

Claim Rejection Under 35 U.S.C. §103

Claims 1-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Maeda et al. (U.S. Patent No. 6,618,455, hereafter Maeda) in view of Sweeney et al. (US 2004/0208568, hereinafter Sweeney) and further in view of Perkins et al (US 2004/0156325, hereinafter Perkins).

INDEPENDENT CLAIM 1

As an example, independent claim 1 recites, among other things, a feature of "the first synchronous state indication code is converted into the second synchronous state indication code by use of a conversion table such that plural values of the first synchronous state indication code different from each other are assigned to respective values of the second synchronous state indication code different from each other." As will be explained below, at least the above-noted

feature of claim 1 is a distinction over Sweeney, and thus over its combination with Maeda and Perkins.

On page 4, the Office Action admits that Maeda does not teach converting the first synchronous state indication code used by the first synchronization scheme into a second synchronous state indication code used by the second synchronization scheme. The Office Action then relies on Sweeney, and contends that Sweeney in paragraphs 0027, 0043, 0062, and Fig. 2 discloses the above-noted code conversion. However, Sweeney discloses in paragraph 0062:

> Also generated within the clock and data recovery loss of signal detection module 24 is a loss-of-signal indication 22 based on the presence of a predetermined number of consecutive logical zeros in the binary data stream or on the absence of a recovered clock signal for a predetermined interval of time. The loss-of-signal 22 is reset after declaration based on the presence of a predetermined number of consecutive logical transitions in the binary data stream 25 or in the presence of a recovered clock signal for a predetermined interval of time.

Namely, Sweeney only suggests detecting a poor quality state of a recovered clock signal (i.e., "presence of a predetermined number of consecutive logical zeros in the binary data stream" or "absence of a recovered clock signal") to generate a state indication signal (i.e., "loss-of-signal 22") and detecting a good quality state of a recovered clock signal (i.e., "presence of a predetermined number of consecutive logical transitions in the binary data stream" or "presence of a recovered clock signal") to reset the state indication signal (i.e., the resetting of the "loss-of-signal 22"). In other words, Sweeney only teaches or suggests generating and resetting a state indication signal based on a state of quality of a recovered clock signal. Sweeney is silent about converting a first synchronous state indication code into a second synchronous state indication code, let alone performing such a conversion by use of a conversion table.

Accordingly, neither Maeda nor Sweeney, taken alone or in combination, teaches or suggests converting a first synchronous state indication code into a second synchronous state indication code by use of a conversion table, such that

plural values of the first synchronous state indication code different from each other are assigned to respective values of the second synchronous state indication code different from each other.

The Office Action on page 6 admits that Maeda-Sweeney fails to teach "such that plural values of the first synchronous state indication code different from each other are assigned to respective values of the second synchronous state indication code different from each other." The Office Action then relies on Perkins, and contends that Perkins discloses this feature in Figs. 3, 4, and 5 and paragraphs 0007, 0016, and 0045. Paragraph 0016 referred to in the Office Action reads in part: "the line side frequency is always the same frequency for the payload signal and the local frequency at a terminal or intermediate node is set to a local reference clock in accordance with the payload type and its overhead ratio (OHR), i.e., the overhead ratio is varied to meet the desired difference between the line rate or frequency and the client signal payload rate for the client signal payload type." This is also described in paragraph 0056, in which Perkins states:

> the essence of this network system is to operate all line sides of the network (i.e., the signal path propagation between node elements) at the same frequency or rate. ... Therefore, the present invention provides for a variable overhead ratio (V-OHR) that changes in accordance with the client signal payload type being received from the line side into a node side with the line rate always remaining a fixed frequency.

Accordingly, Perkins discloses changing the overhead ratio in accordance with the client signal payload type to meet a difference between the line frequency and the local clock frequency. The justification bytes (i.e., NJO-N bytes and PJO-M bytes) shown in Fig. 4 are added to compensate for frequency differences, and represent the required compensation for a frequency difference (see paragraph 0049). It should be noted that the justification bytes merely relate to frequency differences, and are not plural values of the first synchronous state indication code that are assigned to respective values of the second synchronous state indication code different from each other.

Accordingly, none of Maeda, Sweeney, and Perkins, taken alone or in combination, teaches or suggests converting a first synchronous state indication code into a second synchronous state indication code, let alone performing such a conversion by use of a conversion table. Moreover, none of Maeda, Sweeney, and Perkins, taken alone or in combination, teaches or suggests plural values of the first synchronous state indication code different from each other that are assigned to respective values of the second synchronous state indication code different from each other.

Hence, the above-noted feature of claim 1, namely "the first synchronous state indication code is converted into the second synchronous state indication code by use of a conversion table such that plural values of the first synchronous state indication code different from each other are assigned to respective values of the second synchronous state indication code different from each other," is a distinction over the asserted combination of references, i.e., Maeda, Sweeney, and Perkins.

Among other things, a *prima facie* case of obviousness must establish that the asserted combination of references teaches or suggests each and every element of the claimed invention. In view of the distinction of claim 1 noted above, at least one claimed element is not present in the asserted combination of references. Hence, the Office Action fails to establish a *prima facie* case of obviousness vis-à-vis claim 1. Claims 2-3 ultimately depend from claim 1, respectively, and so at least similarly distinguish over the asserted combination of references.

INDEPENDENT CLAIM 4

As an example, independent claim 4 recites, among other things, a feature of "the conversion of the synchronous state indication code is performed by use of a conversion table such that plural values of the synchronous state indication code different from each other used by said other one of the first synchronization scheme and the second synchronization scheme are assigned to respective values of the

synchronous state indication code different from each other used by said given one of the first synchronization scheme and the second synchronization scheme."

As previously described, none of Maeda, Sweeney, and Perkins, taken alone or in combination, teaches or suggests converting a first synchronous state indication code into a second synchronous state indication code by use of a conversion table, let alone plural values of the first synchronous state indication code different from each other that are assigned to respective values of the second synchronous state indication code different from each other. Hence, the above-noted feature of claim 4 is a distinction over the asserted combination of references, i.e., Maeda, Sweeney, and Perkins.

Claims 5-9 ultimately depend from claim 4, respectively, and so at least similarly distinguish over the asserted combination of references.

In view of the foregoing discussion, the rejection of claims 1-9 is improper. Accordingly, withdrawal of the rejection is respectfully requested.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below.

Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 50-4610.

Respectfully submitted,

Dated: August 6, 2010

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